AMENDMENTS TO THE CLAIMS

1-16. (canceled)

17. (currently amended) A method of forming a capacitor, comprising:

forming an in-laid conductor structure on a substrate~~;~~, the in-laid conductor structure ~~including~~ formed in an intra-layer dielectric;

forming ~~a first~~ an electrode layer ~~over~~ directly on the conductor structure;

forming a ~~second~~ first layer over the ~~first~~ electrode layer;

forming a ~~third~~ second layer over the ~~second~~ first layer;

forming a patterned masking layer over the ~~third~~ second layer such that a portion of the ~~third~~ second layer is exposed, and patterning the ~~third,~~ second, ~~and~~ first and electrode layers in alignment with the masking layer, so as to form a vertical stack superjacent the conductor structure; and

forming a second conductor over the vertical stack.

18. (currently amended) The method of Claim 17, wherein the ~~first~~ electrode layer comprises tantalum, the ~~second~~ first layer comprises tantalum pentoxide, and the ~~third~~ second layer comprises tantalum.

19. (original) The method of Claim 18, wherein the in-laid conductor and the second conductor comprise copper.

20. (currently amended) The method of Claim 17, wherein forming the ~~first~~ electrode layer comprises depositing tantalum.

21. (currently amended) The method of Claim 17, wherein forming the ~~second~~ first layer comprises depositing tantalum pentoxide.

22. (currently amended) The method of Claim 21, wherein forming the ~~third~~ second layer comprises depositing tantalum.

23. (currently amended) The method of Claim 17, further comprising forming an electrically insulating layer over the ~~third~~ second layer and patterning the insulating layer so as to expose portions of the ~~third~~ second layer prior to forming the second conductor.

24. (currently amended) The method of Claim 23, wherein forming a second conductor over the vertical stack includes making electrical contact between the second conductor and the ~~third~~ second layer.

25. (withdrawn) A method of forming a capacitor, comprising:

forming a plurality of in-laid conductors on a substrate;

selectively depositing a first conductive material over the plurality of in-laid conductors;

blanket depositing a layer of high-k dielectric material over the substrate;

blanket depositing a second conductive material over the high-k dielectric material; and

patterning the second conductive material and the high-k dielectric material.

26. (withdrawn) The method of Claim 25, wherein patterning the second conductive material and the high-k dielectric material comprises etching the second conductive material and the high-k dielectric material such that they are removed from a portion of the underlying plurality of in-laid conductors.

27. (withdrawn) The method of Claim 26, wherein the in-laid conductors comprise copper.

28. (withdrawn) The method of Claim 27, wherein the first and second conductors comprise tantalum and the high-k dielectric material comprises tantalum pentoxide.

29. (withdrawn) The method of Claim 27, wherein the high-k dielectric material comprises barium strontium titinate.

30. (withdrawn) A method of forming a capacitor, comprising:

forming a plurality of in-laid conductors on a substrate;

blanket depositing a first conductive material over the plurality of in-laid conductors;

blanket depositing a layer of high-k dielectric material over the substrate;

blanket depositing a second conductive material over the high-k dielectric material;

blanket depositing a third conductive material over the second conductive material;

forming a patterned layer of photoresist over the third conductive material so as to expose portions of the third conductive material;

etching the exposed portions of the third conductive material and removing the photoresist; and

etching the second conductive material, the high-k dielectric layer, and the first conductive material, using the third conductive material as a hardmask.

31. (withdrawn) The method of Claim 30, wherein the third conductive material comprises aluminum, and etching the second conductive material, the high-k dielectric layer, and the first conductive material comprises etching with a fluorine based plasma.

32. (withdrawn) The method of Claim 31, wherein the high-k dielectric comprises an oxide of tantalum.

33. (withdrawn) The method of Claim 30, wherein the third conductive material comprises tungsten, and etching the second conductive material, the high-k dielectric layer, and the first conductive material comprises etching with a fluorine based plasma.

34. (withdrawn) The method of Claim 33, wherein the high-k dielectric comprises barium strontium titinate.

35. (withdrawn) The method of Claim 32, wherein the first conductive material is a barrier to copper diffusion.

36. (withdrawn) The method of Claim 34, wherein the first conductive material is a barrier to copper diffusion.

37. (new) A method, comprising:

forming a first conductor structure in an inter-layer dielectric (ILD);

forming a bottom electrode layer directly on the first conductor structure, the bottom electrode layer consisting essentially of a material selected from the group consisting of tantalum nitride (TaN), titanium nitride (TiN), tungsten nitride (WN) and ruthenium (Ru);

forming a dielectric layer directly on the bottom electrode layer;

forming a top electrode layer directly on the dielectric layer; and

forming a second conductor structure over the top electrode layer.

38. (new) The method of claim 37, wherein forming the bottom electrode layer comprises selectively plating said material selected from the group consisting of TaN, TiN, WN and Ru onto the first conductor.

39. (new) The method of claim 37, wherein forming the bottom electrode layer comprises:

depositing a polycrystalline film of the TaN or TiN; and

selectively etching grain boundaries of the film with a wet chemical etch.

40. (new) The method of claim 37, wherein the dielectric layer is barium strontium titinate (BST) or tantalum pentoxide (Ta_2O_5).

41. (new) The method of claim 37, wherein the top electrode layer consists essentially of a material selected from the group consisting of Ru, TaN, TiN, WN, platinum (Pt) and iridium (Ir).

42. (new) The method of claim 37, further comprising:

forming a hardmask layer over the top electrode layer;

forming a photoresist layer over the hardmask layer;

patterning the photoresist layer to expose a portion of the hardmask layer;

etching the exposed portion of the hardmask layer using a fluorine based etchant to expose a portion of the top electrode layer;

removing the photoresist layer by ashing; and

etching the exposed portion of the top electrode layer and the dielectric and bottom electrode layer directly under the exposed portion of the top electrode layer to form a capacitor stack, wherein the second conductor structure is formed over the top electrode layer of the capacitor stack.

43. (new) The method of claim 37, further comprising:

forming a nitride layer over the top electrode layer;

forming a second ILD over the nitride layer;

forming a via in the second ILD to expose a portion of the nitride layer;

etching the exposed portion of the nitride layer to expose a portion of the top electrode layer;

forming a conductive barrier layer over exposed surfaces of the via; and

filling the via with a conductive material to form the second conductor structure.

44. (new) A method, comprising:

forming a first conductor structure in an inter-layer dielectric (ILD);

forming a bottom electrode layer directly on the first conductor structure, the bottom electrode layer consisting of a layer of conductive material that substantially prevents diffusion of oxygen, oxygen-containing compounds and copper;

forming a dielectric layer directly on the bottom electrode layer;

forming a top electrode layer directly on the dielectric layer; and

forming a second conductor structure over the top electrode layer.

45. (new) The method of claim 44, wherein the bottom electrode layer is textured.

46. (new) The method of claim 44, wherein the dielectric layer has a dielectric constant greater than that of silicon dioxide.

47. (new) The method of claim 44, wherein the ILD is silicon dioxide, carbon doped oxides of silicon, fluorine doped oxides of silicon, porous oxides of silicon or organic polymers.

48. (new) The method of claim 44, wherein the top electrode layer consists essentially of a material selected from the group consisting of Ru, TaN, TiN, WN, platinum (Pt) and iridium (Ir).

49. (new) The method of claim 44, further comprising:

forming a photoresist layer over the top electrode layer;

patterning the photoresist layer to expose a portion of the top electrode layer;

etching through the exposed portion of the top electrode layer and the dielectric and bottom electrode layer directly under the exposed portion of the top electrode layer;

stripping the photoresist layer;

forming an etch stop layer over exposed surfaces of the ILD, bottom electrode layer, dielectric layer and top electrode layer;

forming a second ILD over the etch stop layer; and

forming the second conductor structure in the second ILD.